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10/776,460	02/10/2004	Sameer Kanagala	HAMMP006	3496

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EXAMINER	
LAI, ANDREW	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,460	KANAGALA ET AL.	
	Examiner	Art Unit	
	ANDREW LAI	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,10,12-14,23,25-29,32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sutoh et al (US 2003/0165115, Suhoh hereinafter) in view of Sha (US 6,868,057) and further in view of Natarajan et al (US 2004/0086003, Natarajan hereinafter).

- **With respect to independent claims 1, 13, 26, 27, 28, 31 and 34**

Sutoh discloses "a hitless switching system includes a sending apparatus and a receiving apparatus" (Abstract lines -2) comprising the following features.

Regarding claims 1, 26 and 28, *a method of protecting a protected egress link* (see "according to this invention, for example, a protection transmission line transmitting second signal can be commonly used by a plurality of working transmission lines (transmitting first signal)", [0046] lines 1-4, wherein "protection transmission line" is "between the second sending interface and the second receiving interface", [0125] lines 1-3, and "working transmission line" is "between the first sending interface and the first receiving interface", [0125] lines 4-6) *including…*

Claim 1, *connecting traffic from a service module* (fig. 7 "client interface 590" in conjunction with "distributing part", "SM_e" hereinafter) *to a first physical module* (fig. 7 top half second [downward direction] "branch part", "PM1_e" hereinafter, right to and receiving traffic from said "SM_e", and see "signals are branched by the branch part", [0130] lines 7-8) *that is connected to the protected egress link* (fig. 7 "sending interface 530" outputting egress traffic from "PM1_e"),

connecting the traffic through the first physical module (refer to fig. 7 and see traffic out of said "PM1_e") *through a pooling switch* (fig. 7 "multiplexing part 520", "PS_e" hereinafter, right to and receiving traffic from "PM1_e") *to a second physical module* (fig. 7 "sending interface 540", "PM2_e" hereinafter, right to and receiving traffic from "PS_e") *that is connected to an alternate egress link* (fig. 7 egress link out of "PM2_e").

Claim 26, *connecting traffic from a service module* (fig. 7 "client interface 590", "SM_e" hereinafter) *to a first pooling switch* (fig. 7 top half "distributing part", "PS1_e" hereinafter, right to and receiving traffic from said "SM_e");

connecting the first pooling switch ("PS1_e") *to a first physical module* (fig. 7 top half second [downward direction] "branch part", "PM1_e" hereinafter, right to and receiving traffic from said "PM1_e", and see "signals are branched by the branch part", [0130] lines 7-8) *that is connected to a protected egress link* (fig. 7 "sending interface 530" outputting traffic from "PM1_e");

connecting the traffic through the first physical module (refer to fig. 7 and see traffic out of said "PM1_e") *through a second pooling switch* (fig. 7 "multiplexing part

520", "PS2_e" hereinafter, right to and receiving traffic from "PM1_e") *to a second physical module* (fig. 7 "sending interface 540", "PM2_e" hereinafter, right to and receiving traffic from "PS2_e") *that is connected to an alternate egress link* (fig. 7 egress link out of "PM2_e").

Claim 28, *connecting traffic from a service module* (fig. 7 "client interface 590", "SM_e" hereinafter) *to a first pooling switch* (fig. 7 top half "distributing part", "PS1_e" hereinafter, right to and receiving traffic from said "SM_e"),

connecting the first pooling switch ("PS1_e") *to a first physical module* (fig. 7 top half second [downward direction] "indicator providing part", "PM1_e" hereinafter, right to and receiving traffic from said "PM1_e");

connecting the traffic through the first physical module through a second pooling switch (fig. 7 top half second [downward direction] "branch part", "PS2_e" hereinafter, right to and receiving traffic from said "PM1_e") *to a second physical module* (fig. 7 "multiplexing part 510", "PM2_e" hereinafter, right to and receiving traffic from said "PS2_e") *that is connected to the protected egress link* (fig. 7 egress link out of "sending interface 530", which is right to and receiving traffic from said "PS2_e");

connecting the traffic through the first physical module ("PM1_e" above) *through the second pooling switch* ("PS2_e" above) *to a third physical module* (fig. 7 "multiplexing part 520", "PM3_e" hereinafter, right to and receiving traffic from "PS2_e") *that is connected to an alternate egress link* (fig. 7 egress link out of "sending interface 540").

Regarding claims 13, 27 and 31, *a method of protecting a protected ingress link* (see "according to this invention, for example, a protection transmission line transmitting second signal can be commonly used by a plurality of working transmission lines (transmitting first signal)", [0046] lines 1-4, wherein "protection transmission line" is "between the second sending interface and the second receiving interface", [0125] lines 1-3, and "working transmission line" is "between the first sending interface and the first receiving interface", [0125] lines 4-6) *including…*

Claim 13, *connecting traffic to a service module* (fig. 7 "client interface 595" in conjunction with "restoration part", "SM_i" hereinafter) *from a first physical module* (fig. 7 bottom half last [downward direction] "selector", "PM1_i" hereinafter, left to and sending traffic to said "SM_i", and see "selectors each of which selects one signal from a plurality of signals", Abstract lines 10-11) *that is connected to the protected ingress link* (fig. 7 "receiving interface 550" inputting ingress traffic to "PM1_i"),

connecting the traffic through a second physical module (fig. 7 bottom half "receiving interface 560", "PM2_i" hereinafter, left to and sending through traffic to "PM1_i") *that is connected to an alternate ingress link* (fig. 7 ingress link to said "PM2_i") *through a pooling switch* (fig. 7 "demultiplexing part 580", "PS2_i" hereinafter, right to and receiving through traffic from said "PM2_i") *to the first physical module* (fig. 7 showing said "PS2_i" passing traffic to said "PM1_i").

Claim 27, *connecting traffic to a service module* (fig. 7 "client interface 595", "SM_i" hereinafter) *from a first pooling switch* (fig. 7 bottom half "restoring part", "PS1_i" hereinafter, left and sending traffic to "SM_i"),

connecting the first pooling switch ("PS1_i") *to a first physical module* (fig. 7 bottom half last [downward direction] "selector", "PM1_i" hereinafter, left to and sending traffic to said "PS1_i", and see "selectors each of which selects one signal from a plurality of signals", Abstract lines 10-11) *that is connected to a protected ingress link* (fig. 7 "receiving interface 550" inputting traffic to "PM1_i"),

connecting the traffic through a second physical module (fig. 7 bottom half "receiving interface 560", "PM2_i" hereinafter, passing through traffic) *that is connected to an alternate ingress link* (fig. 7 ingress link to said "PM2_i") *through a pooling switch* (fig. 7 "demultiplexing part 580", "PS2_i" hereinafter, right to and receiving through traffic from "PM2_i") *to the first physical module* (fig. 7 showing said "PS2_i" passing traffic to said "PM1_i").

Claim 31, *connecting traffic to a service module* (fig. 7 "client interface 595", "SM_i" hereinafter) *from a first pooling switch* (fig. 7 bottom half "restoring part", "PS1_i" hereinafter, left of and pooling traffic to "SM_i");

connecting the first pooling switch ("PS1_i") *to a first physical module* (fig. 7 bottom half last [downward direction] "selector", "PM1_i" hereinafter, left of and passing through traffic to said "PS1_i");

connecting the traffic through a second physical module (fig. 7 "demultiplexing part 570", "PM2_i" hereinafter, left of and passing through traffic to "PS2_i") *that is connected to a protected ingress link* (fig. 7 "receiving interface 550" left of and passing ingress traffic to "PM2_i") *through a second pooling switch* (fig. 7 bottom half, the combination of "phase control part" and the last [downward direction] "elastic store

memory", "PS2_i" hereinafter, left of and passing through traffic to "PM1_i") *to the first physical module* ("PM1_i" above).

Regarding claim 34, *a device for switching traffic* (see "a hitless switching system", Abstract line 1) *comprising:*

a first pooling switch (fig. 8 "switch part 810" and "multiplexing part 610") *configured to be connected to a plurality of physical modules* (fig. 8 "sending interface 620"),

a frame passing module (fig. 8 the top pair "indicator providing part" and "branch part", "FPM" hereinafter, and noting "the distributing part includes:", [0047] line 2 "a part for inserting H4 byte multi-frame into each virtual concatenation signal", [0049], which frame as shown in fig. 8 is passed to said "FPM" and further to "switch part 810") *connected to the first pooling switch* (fig. 8 depicting "FPM" connected to "switch part 810),

a second pooling switch (fig. 8 "distributing part") *connected to the* frame passing module (fig. 8 depicting "distributing part" connected to the "FPM"),

a service module (fig. 8 "client interface 660") *connected to the second pooling switch* (fig. 8 depicting "client interface 660" connected to "distributing part").

Regarding the feature of "*having a link layer framer* " [in the first physical module] for claims 1, 13, 26, 27, 28 and 31, and "*a link layer frame module*" connected to the first pooling switch for claim 34, Sutoh suggests such framer in the "distribution part" (refer to fig. 7 and see "the distributing part includes:", [0047] line 2 and "a part for inserting H4 byte multi-frame in to each virtual concatenation signal", [0049]). Sutoh

however does not disclose, regarding claims 1, 13, 26, 27, 28 and 31, a first physical module ("PM1_e" for claims 1/26/28 and "PM1_i" for claims 13/27/31) "*having a link layer framer, wherein the link layer framer includes a queue for storing the traffic*"; regarding claim 34, "*a link layer framer*" connected to the first pooling switch and a second pooling switch connected to "*the link layer framer*".

However, using *link layer framer* with *queue* or buffer is an old and well-known technique in the field of protection lines/switches. There are numerous such disclosures, of which Sha is one example.

Sha discloses a "automatic protection switch decision engine" (col. 1 lines 1-2) which "decides to assign a service line to be active or in standby mode" (Abstract lines 1-2). Sha's invention comprises:

Regarding claims 1, 13, 26, 27, 28 and 31, a first physical module ("PM1_e" for claims 1/26/28 and "PM1_i" for claims 13/27/31 in the case of Sutoh, and in the case of Sha, e.g., "module 30" or "module 50" in fig. 2 depending on egress/ingress directions) *having a link layer framer, wherein the link layer framer includes a queue for storing the traffic* (refer to fig. 2 "module 30/40", see, e.g. "framer 111/115" and see further, in view of fig. 3 step 304, "CPU 156 makes decisions about what actions, if any, should be applied to buffers of framers 111 and 115", col. 4 lines 35-37, and it is well known in the art that buffers or *queues* are used *for storing traffic* or data).

Regarding claim 34, *a link layer framer* (fig. 2, e.g. "framer 111" connected to the first pooling switch (fig. 2, e.g. "ATM proc. unit 140") and a second pooling switch

(fig. 2, e.g. "LIU [line interface unit] 110") connected to *the link layer framer* ("framer 111").

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method/device of Sutoh by adding the link layer and associated buffers of Sha to Sutoh in order to provide a simpler and yet effective system "with a very simple decision logic" (Sha, col. 3 lines 3-4) to overcome the complexity of prior arts using state machine which "is quite large" (Sha, col. 2 lines 62) that "can slow down performance and certainly increases the cost of maintenance" (Sha, col. 2 lines 65-67).

Sutoh in view of Sha, however, does not disclose, regarding claims 1, 13, 26, 27, 28 and 31, wherein the traffic in the second physical module *is not processed through any link layer framer*; and regarding claim 34, wherein each of the plurality of physical modules is configured *to not process traffic through a link layer framer.*

However, whether or not to pass/process *traffic through a link layer framer* is well known in the art to depend on process necessity, which has been a well established technique familiar to one skilled in the art. One example of such technique can be seen in Natarajan.

Natarajan discloses "a multirate transceiver wherein data can be received at a first data rate and transmitted at a second data rate" (Abstract lines 1-3), which system comprises, in view of figs. 2 through 9 especially figs. 2 and 4, "both the ingress path 205a and the egress path 205b" ([0032] lines 1-2) and the "ingress path 205a/205b" has "framer 228a/228b". Natarajan particularly discloses:

Regarding claims 1, 13, 26, 27, 28 and 31, wherein the traffic in the second physical module *is not processed through any link layer framer*;

Regarding claim 34, wherein each of the plurality of physical modules is configured *to not process traffic through a link layer framer.*

(refer to figs. 2/4 for ingress/egress and see "a bypass route is included for bypassing the mapper 225a/225b when mapping is not desired. In an alternate embodiment, both the framer 228a/228b and mapper 225a/225b can be bypassed", [0041/0046] lines 1-4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method/device of Sutoh by adding the framer bypassing feature of Natarajan to Sutoh in order to provide a more robust system that "would be advantageous to provide a more flexible scheme for accommodation of the varying user requirements" (Natarajan, [0008] lines 1-3).

- **With respect to dependent claims**

Sutoh discloses the following features:

Regarding claims 10/23, *wherein the pooling switch enables multiple logical streams to be included in one physical interface* (see "a receiving part for receiving virtual concatenation signals, wherein the virtual concatenation signals are obtained by dividing an original signal into virtual concatenation signals", [0054] lines 1-4).

Regarding claims 12/25, *wherein pooling switch is a time division multiplexing switch* (fig. 7 depicting, for claim 12, "multiplexing part 520" and, for claim 25, "demultiplexing part 580").

Regarding claims 29/32, *wherein the first physical module* ("PM1_e"/"PM1_i" for claims 29/32, which are discussed in claims 28/31 above) *does not include a link interface module* (note that said "PM1_e"/"PM1_i" are connected to "PS1_e"/"PS1_i" on one end and "PS2_e"/"PS2_i" on the other with no direct linking to an "egress/ingress" link).

Sha discloses the following features:

Regarding claim 14, *wherein the service module* (fig. 2 "ATM switch fabric 100") *decides from information within an input traffic stream to the service module* (refer to fig. 2 and see "two payload data streams are created from the data of framer 117... One of the streams is addressed to framer 111 in I/O module 30, and the other stream is addressed to framer 115 in I/O module 140. The two streams pass through ATM switch 100 [*service module*]", col. 4 lines 8-14) *where to output the input traffic stream* (still refer to fig. 2 and see, continue from above cited texts, "and, thus the information is delivered to framers 111 and 115 and flows out of fibers 210 and 230", col. 4 lines 14-15, noting that for the two streams to be routed to the appropriate framers, "ATM switch 100 [*service module*] must be able to *decide* appropriately *where to output* each *input traffic stream from the* addressed *information with* each *input traffic stream*).

3. Claims 2-7,11,15-20,24,30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sutoh in view of Sha and Natarajan, as applied to claims 1,13,28 and 31 above, and further in view of Simons et al (US 6,332,198, Simons hereinafter)

Sutoh in view of Sha and Natarajan discloses claimed limitations as discussed above in section 2. Sutoh in view of Sha and Natarajan does not expressly disclose the features in aforesaid claims in the heading of this section.

However, Simons discloses "a method and apparatus for supporting multiple redundancy schemes in a single network device" (Abstract lines 1-3) using "universal port cards (or ports)" (Abstract lines 14 and see also fig. 35A "universal port card" 554a-h and 558a-h in both sending and receiving sides) "where one or more of the ports are primary ports and one or more of the ports may be redundant ports" (col. 5 lines 8-10) comprising the features in aforesaid claims. Particularly, Simons discloses:

Regarding claims 2/3 and 15/16, *wherein the first/second physical module contains an optical interface module* (refer to fig. 36A "port 571a…571n" and see "As one example, port 571a is connected to an ingress optical fiber 576a carrying an OC-48 SONET stream and an egress optical fiber 576a carrying an OC-48 SONET stream", col. 46 lines 59-62).

Regarding claims 4/5 and 17/18, *wherein the first/second physical module contains an electrical link interface module* (refer to fig. 36A "SERDES 580a…580n" and see "Port 571a passes optical data from SONET stream on fiber 576a to transceiver 572a. Transceiver 572a converts the optical data into electrical signals that is sends to a SONET framer 574a.", col. 46 lines 62-65 and further "SONET framer 574a sends data over a telecommunications bus 578a to a serializer-deserializer (SERDES) 580a", col. 46 line 66 – col. 47 line 2, noting that said "SERDES 580a" interfaces with "cross

connection card 562a" and thus obvious to one skilled in the art serves as *an electrical link interface module*).

Regarding claims 6/7 and 19/20, *wherein the first/second module contains a module that places the traffic in proper form for a pooling switch* (refer to fig. 36A and see "a serializer-deserializer (SERDES) 580a that serializes the data into four serial lines with twelve STS-1 time slots each and transmits the four serial lines to cross-connect card 562a", col. 47 lines 1-4).

Regarding claims 11 and 24, *wherein the pooling switch is a packet switch* (refer to fig. 36A and see "The sonnet framer organizes the data it receives from the transceiver into SONET frames. SONET framer 574a sends data over a telecommunications bus 578a to a serializer-deserializer (SERDES) 580a that serializes the data ... and transmits the four serial lines to cross-connect card 562a", col. 46 line 66 – col. 47 line 4, noting that SONET frames comprise packets and thus it is obvious to one skilled in the art that cross-connect card 562a, equivalent to said *pooling switch,* will have to be a packet switch in order to be able to handle the SONET frames).

Regarding claims 30 and 33, *wherein 1:N protection is provided* (see "The present invention provides a method and apparatus for supporting multiple redundancy schemes in a single network device. In one network device, various redundancy schemes are supported including 1:1, 1+1, 1:N", Abstract lines 1-4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of Sutoh by adding the various features of Simons, including optical/electronic interfaces, packet switching and 1:N redundancy, to

Sutoh in order to formulate a more robust mechanism that "provides network managers with maximum flexibility in choosing redundancy schemes for their network devices" (Simons, col. 2 lines 51-53).

4. Claims 8-9 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sutoh in view of Sha and Natarajan, as applied to claims 1 and 13 above, and further in view of Sawey et al (US 6,195,330, Sawey hereinafter).

Sutoh in view of Sha and Natarajan described claimed limitations as discussed above for claims 1 and 13. Sutoh in view of Sha and Natarajan does not expressly disclose the features in aforesaid claims in the heading of this section.

However, Sawey discloses a "method and system for hit-less switching" (col. 1 lines 1-2) with "The capability to hit-less switch between redundant paths, such as working channel 7 [fig. 2] and protect channel 9" (col. 4 lines 57-58) wherein "a second digital signal in which a second payload identical to the first payload, a second payload indicator marker and a second overhead are transported on a second channel" (col. 2 lines 51-54) comprising the features of aforesaid claims. Particularly, Sawey discloses:

Regarding claims 8/21, *wherein the traffic through the protected egress link and a protecting egress/ingress link have a synchronization difference smaller than 50ms;*

Regarding claims 9/22, *wherein the traffic through the protected egress link and a protecting egress/ingress link behave in a manner to the user as if there is no synchronization difference between the two traffic flows.*

(see "Payload indicator markers indicating the start of their corresponding payloads are sent to each elastic buffer every frame. At the elastic buffer outputs, the monitor circuit determines the time difference between the appearance of the two payload indicator markers, which corresponds to the difference in network delay between the two copies of the payload. The read counter for the protect traffic instantaneously adjusts for the amount of the delay between the two payload indicator markers", col. 3 lines 11-19. It is obvious to one skilled in the art that Sawey discloses a full synchronization between the traffic flows on working and the protect channel, and as such, *have a synchronization difference smaller than 50ms,* and *to the user as if there is no synchronization difference between the two traffic flows*)

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method/system of Sutoh by adding the synchronization method of Sawey to Sutoh in order to provide an easier synchronization that in turn "provides the capability to perform a hit-less switch between two signals without having to first frame align the two signals and which is therefore simpler and less costly than present hit-less switching techniques" (Sawey, col. 3 lines 41-44).

Response to Arguments

5. Applicant's arguments with respect to all of the independent claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments are drawn to the newly added features in various independent claims by stating (Remarks, page 9 third paragraph) "With respect to claims 1, 13, 26-28, 31, and 34, neither Sutoh nor Simmons teach or disclose having a

first physical module that includes a link layer framer, 'wherein link layer framer includes a queue for storing the traffic,' and a second physical module, 'wherein the traffic in the second physical module is not processed through any link layer framer.'"

As presented above in section 2, newly found art of Sha clearly teaches link layer framer having a buffer (queue) therein for storing traffic and newly found art of Natarajan clearly provides traffic bypassing a framer (traffic not processed through a framer) when desired.

Applicant's other arguments are not addressed herein because they are entirely based on the dependencies on the base claims of which applicant's arguments have been addressed hereinabove.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW LAI whose telephone number is (571)272-9741. The examiner can normally be reached on M-F 7:30-5:00 EST, Off alternative Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2616

/Andrew Lai/
Examiner, Art Unit 2616